User Manual

MSC MPW10K2

Version: 1.1

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Contents

1 Features

Channels:	TDC-Core 10K2, implemented as hardmacro with one Start- and one Stop-input, both inputs trigger on rising edges, separated power supply for the core
Typ. resolution:	45 ps @ 5V 60 ps @ 3.3V
Typ. measurement range:	5 ns - 10 µs @ 5V 8 ns - 13 µs @ 3.3V
Technology:	0.6µ CMOS standard-cell technology, qualified for MIL 883 (5V ± 10%, -55°C - 125°C)
Voltage range:	2.7 V - 5.5 V
Temperature range:	-40°C - 85°C
Calibration clock:	external oscillator clock: 500 kHz – 20 MHz, programmable division factors: 1, 2, 4 or 8
Calibration:	stand alone measurements of one and two periods of the divided calibration clock
Processor interface:	8 bit data bus / 5 bit address bus
Configuration:	programmable via processor interface
Flash-ALU:	calculates the result of the measurement
Memory:	48 bit result of one measurement
Package:	CQFP44 with 0.8 mm pitch

2 Block Diagram

Figure 2.1 shows the block diagram of the MPW10K2.

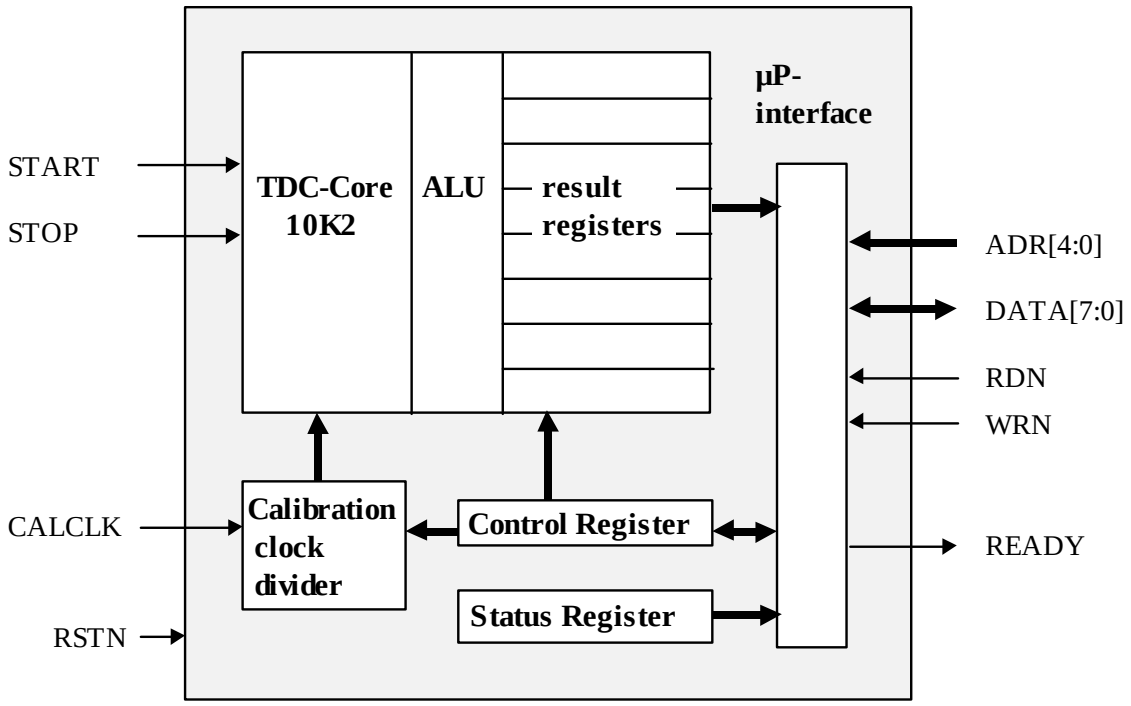


Figure 2.1: MPW10K2 Block Diagram

The measuring core of the MPW10K2 is realised as hardmacro **TDC-Core 10K2** with one Start- and one Stop-input for time measurement between a rising edge of the start-signal at the start-input START and the following rising edge at the stop-input STOP. The measurement result is calculated within the **ALU** and stored in the **result registers**. The result registers can be read out via the **processor interface**.

The configuration of the MPW10K2 is done by writing the **Control Register** via the processor interface. Status information can be accessed by reading the **Status Register**.

The calibration clock, necessary for calibration the time measurement results, has to be supplied by an externally generated quartz oscillator clock at the input CALCLK. The calibration clock is divided by the internal **calibration clock divider** circuit.

3 Package and Pin Configuration

3.1 Package

Figure 3.1 shows the chip's Ceramic Quad Flat Package with 44 pins (CQFP44) and 0,8 mm pitch. The package dimensions are specified in Table 3.1.

The chip's marking is ´MSC MPW10K2 V1.1´.

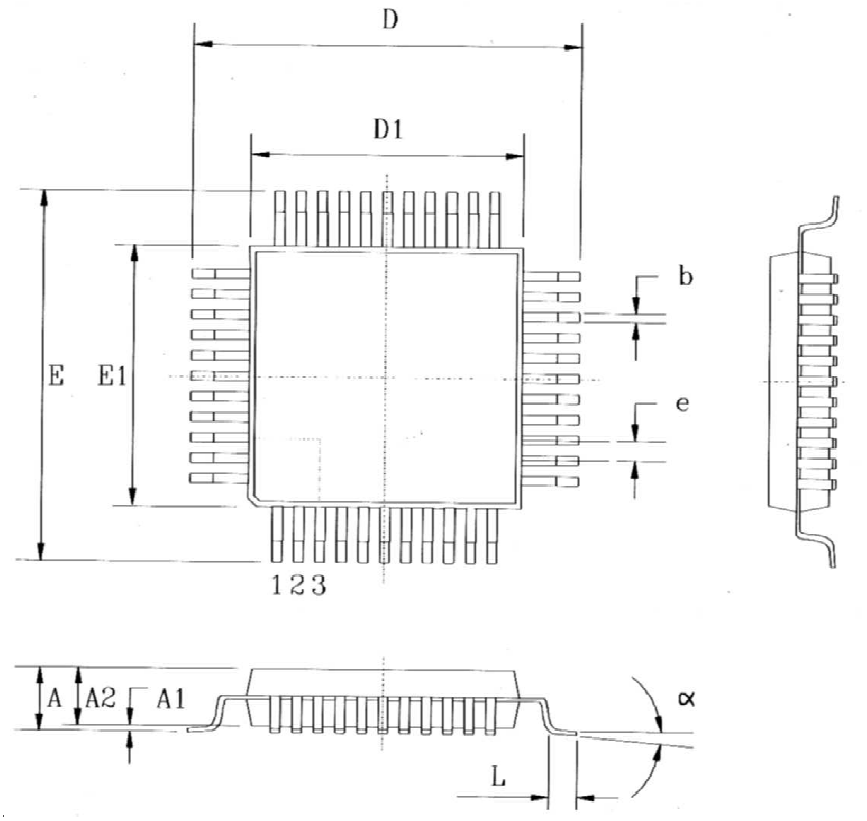


Figure 3.1: Package

	E1 / D1	A	A1	A2	e	b	L	α	D / E	Copl.
min	9,90					0,30	0,60		13,60	
typ		3,10	0,18	2,90	0,80					
max	10,10					0,40	1,00	10°	14,20	0,10

Table 3.1: Package Dimensions [mm]

3.2 Pin Configuration

Table 3.2 shows the MPW10K2's pin configuration. Pin names of low active signals end with 'N'.

Pin No.	Pin name	I/O	Function
5, 7, 35	VDD_I	-	Power supply for internal logic
2, 6, 12, 36, 38	GND_I	-	Ground for internal logic
28, 39	VDD_R	-	Power supply for Inputs
27, 40	GND_R	-	Ground for Inputs
10, 17	VDD_O	-	Power supply for Outputs
11, 18	GND_O	-	Ground for Outputs
42, 44	VDD_C	-	Power supply for measuring core TDC-Core 10K2
37, 43	GND_C	-	Ground for measuring core TDC-Core 10K2
1	RSTN	In	Power-on reset (low active)
3	CALCLK	In	Input for calibration clock: 500 kHz - 20 MHz
13	DATA0	Bidi, 4mA	Bit0 data bus
14	DATA1	Bidi, 4mA	Bit1 data bus
15	DATA2	Bidi, 4mA	Bit2 data bus
16	DATA3	Bidi, 4mA	Bit3 data bus
19	DATA4	Bidi, 4mA	Bit4 data bus
20	DATA5	Bidi, 4mA	Bit5 data bus
21	DATA6	Bidi, 4mA	Bit6 data bus
22	DATA7	Bidi, 4mA	Bit7 data bus
23	ADR0	In	Bit0 address bus
24	ADR1	In	Bit1 address bus
25	ADR2	In	Bit2 address bus
26	ADR3	In	Bit3 address bus
29	ADR4	In	Bit4 address bus
30	RDN	In	Read strobe (low active)
31	WRN	In	Write strobe (low active)
32	START	In	Start-input
33	READY	Out, 4mA	When READY 0 -> 1 the measurement has finished. After 10ns (5V, 25°C) the measurement results are accessible via the result registers at the latest.
41	STOP	In	Stop-input
4, 8, 9, 34	NC		Not connected

Remarks:

- *All inputs are CMOS.*
- *Data bus DATA[7:0] is not allowed to float: please pull up or down (with e.g. 10kΩ).*
- *Do not connect unused outputs.*

Table 3.2: Pin Function List

4 Measuring procedure

The MPW10K2 provides the measuring core TDC-Core 10K2 with a typical resolution of 45ps at 5V and 25°C. The core is realised as hardmacro.

As shown in Figure 4.1, one rising edge-sensitive start-input and one rising edge-sensitive stop-input are available for measuring the time differences $\mathbf{t_{VAL}}$. The *time measurement* in the measuring core is started by a start on the start-input and ended by a stop on the stop-input. The internal ALU calculates the measurement result, consisting of **CC** (Coarsecount), **FC** (Finecount) and **M0** (TDC-specific characteristic quantity), which is stored into the result registers. CC, FC and M0 are required for external calculation of the measurement value **VAL**.

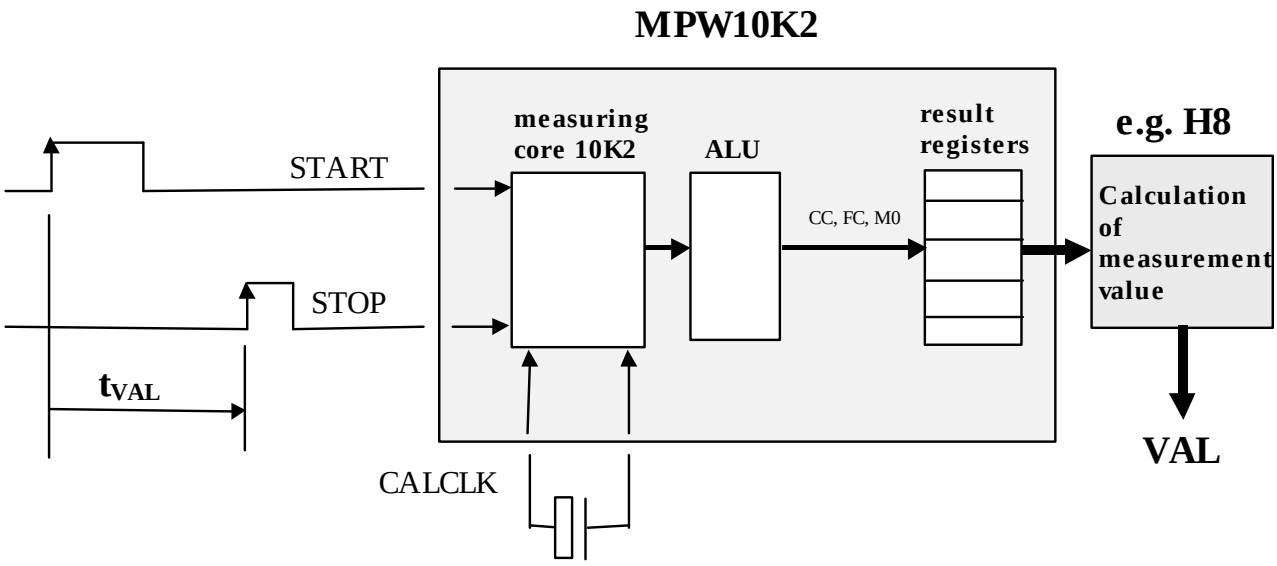


Figure 4.1: Time Difference Measurement

The measurement value VAL is dependent on the temperature and the supply voltage. It therefore has to be weighted according to the TDC characteristic (measurement straight, Figure 4.2). Offset and grade of the characteristic have to be determined by a so-called *calibration measurement*. This can be executed immediately after every time measurement.

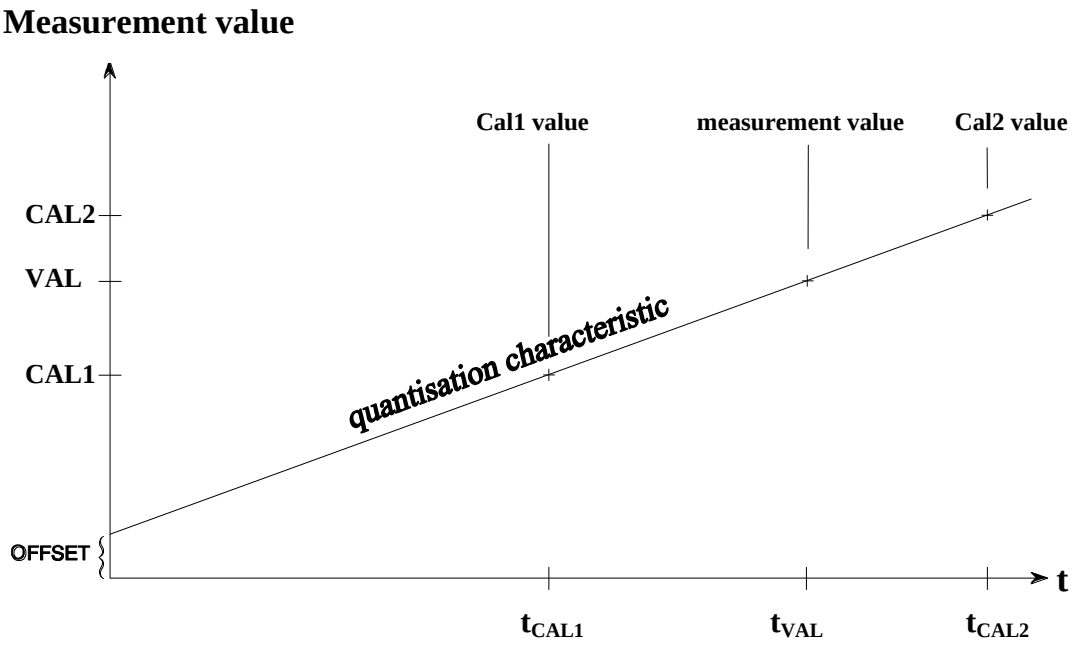


Figure 4.2: Characteristic of the TDC Core

4.1 Generating Calibration Values

For calibration measurements a calibration clock has to be provided at the MPW10K2's pin CALCLK. This clock is the absolute time reference and therefore the clock must have the precision of a quartz crystal. The calibration clock is divided by an internal calibration clock divider. The resulting clock CALCLK_I is used as internal reference clock and measured by the measuring core.

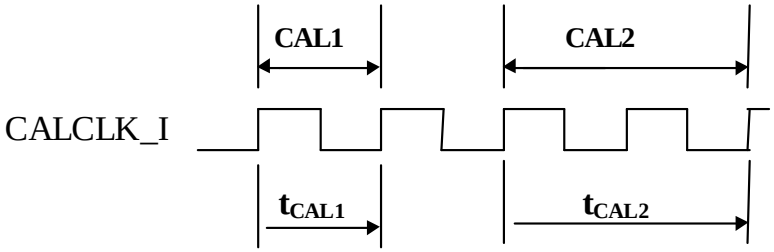


Figure 4.3: Calibration Measurement

During a calibration measurement the length of one and two periods of the divided calibration clock (t_{CAL1}, t_{CAL2}) are measured and the resulting calibration values **CAL1** and **CAL2** (resp. FC, CC and M0 for their external calculation) are stored just like the measurement value VAL (resp. its FC, CC and M0) in the result registers. The time values $\mathbf{t_{CAL1}}$ and $\mathbf{t_{CAL2} = 2 * t_{CAL1}}$ are well known.

A MPW10K2's calibration measurement consists of two successive steps, which have to be activated separately via the Control Register:

1. Generation of calibration value CAL1
2. Generation of calibration value CAL2

4.2 M0-Generation

Measurement- and calibration- values (VAL, CAL1, CAL2) are standardized using *the TDC-specific internal characteristic quantity*, called **M0**. M0 is generated automatically after each time and calibration measurement using the measuring core. Via the Control Register it can be selected, whether the measuring core generates M0 with 1-fold, 4-fold, 16-fold or with 32-fold accuracy. The generation of M0 with 32-fold accuracy takes 32 times longer than the generation of M0 with 1-fold accuracy. Thus higher accuracy of M0 causes a longer dead time of the measurement.

It's also possible to suppress the M0-generation at all. However, in order to minimize the influences of temperature and supply voltage and to optimize the precision of measurement, M0-measurements have to be executed in cyclic temporal distances – just like calibration measurements.

4.3 Calculation of measurement and calibration values

The measurement and calibration values VAL, CAL1 and CAL2 (named VALUE in formula (1)) are calculated as follows using the MPW10K2's measurement results CC, FC and M0:

A) Measurements *WITH* M0-generation

(1) VALUE = CC – (A * FC / M0)

M0-accuracy	A
1-fold	1
4-fold	4
16-fold	16
32-fold	32

B) Measurements *WITHOUT* M0-generation

In this case the measurement and calibration values are calculated using formula (1), too. But M0 has to be generated during a former calibration or time measurement and read out.

4.4 Calculation of the measured time difference t_{VAL}

The measured time difference $\mathbf{t_{VAL}}$ is calculated using the clock period time $\mathbf{t_{CAL1}}$ of the divided calibration clock CALCLK_I, the measurement value **VAL** and the calibration values **CAL1** and **CAL2** in accordance with the TDC characteristic (see Figure 4.2) as follows:

$$\textbf{(2)} \quad t_{VAL} = \frac{\textbf{VAL - Offset}}{\textbf{CAL2 - CAL1}} * t_{CAL1}$$

$$\textbf{(3)} \quad \textbf{Offset} = \textbf{2 * CAL1 - CAL2}$$

5 General Measurement Cycle

Figure 5.1 shows the flowchart of a general measurement cycle. At the beginning of a measurement cycle the M0-generation, the M0-accuracy and the division factor of the calibration clock divider have to be specified within the *Control Register*. During this time the channel has to be disabled.

When the channel is enabled the MPW10K2 is ready for time measurement and waits for a start-signal on the start-input START. After start the MPW10K2 waits for a stop-signal on the stop-input STOP.

The end of a measurement is indicated via pin READY and within the *Status Register* as well. After readout the result registers the channel has to be disabled. For another time measurement the channel has to be enabled again.

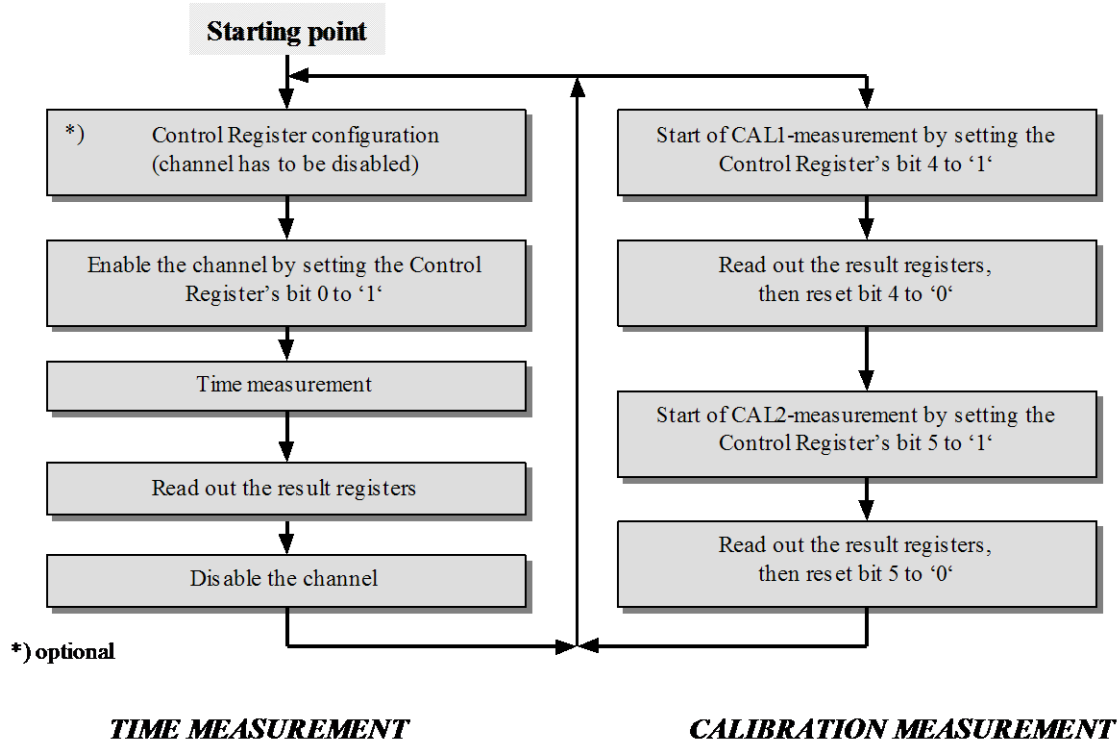


Figure 5.1: General Measurement Cycle Flow

A calibration measurement has to be performed while the channel is disabled. Setting bit 4 of the Control Register to '1' starts the CAL1-measurement. The end of the measurement is indicated via pin READY and within the Status Register. After readout the result registers bit 4 has to be reset to '0'. Then the CAL2-measurement is executed in the same way, setting and resetting the Control Register's bit 5.

6 Functional Description

6.1 Calibration Clock Divider

Figure 6.1 shows the principle function of the calibration clock divider.

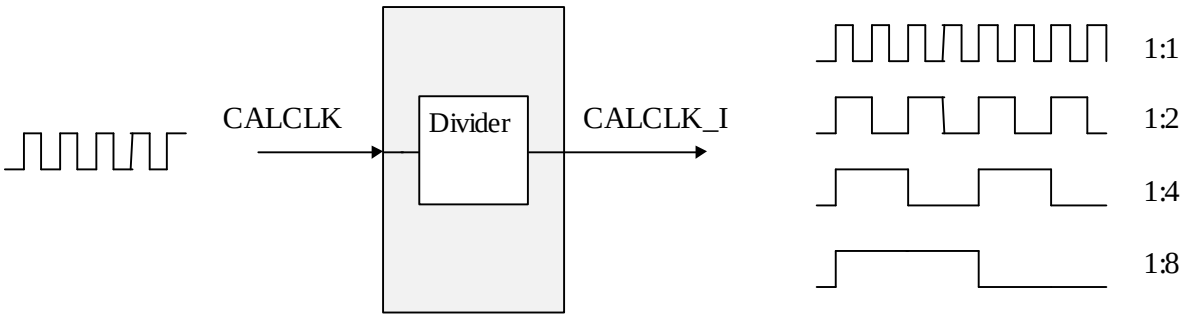


Figure 6.1: Calibration Clock Divider

The external calibration clock CALCLK is divided by the MPW10K2's calibration clock divider. The division factors are programmable and can be 1, 2, 4 or 8.

It is necessary to ensure that the clock period of the divided calibration clock is not larger than 5µs (5V, typ), otherwise the measurement of two calibration clock periods would cause a measurement range overflow within the measuring core.

In order to achieve high precision accuracy the division factor should be selected in such a way, that the time difference t_{VAL} to be measured is between one and two calibration clock periods.

6.2 Measurement Channel

Figure 6.2 shows the block diagram of the measurement channel.

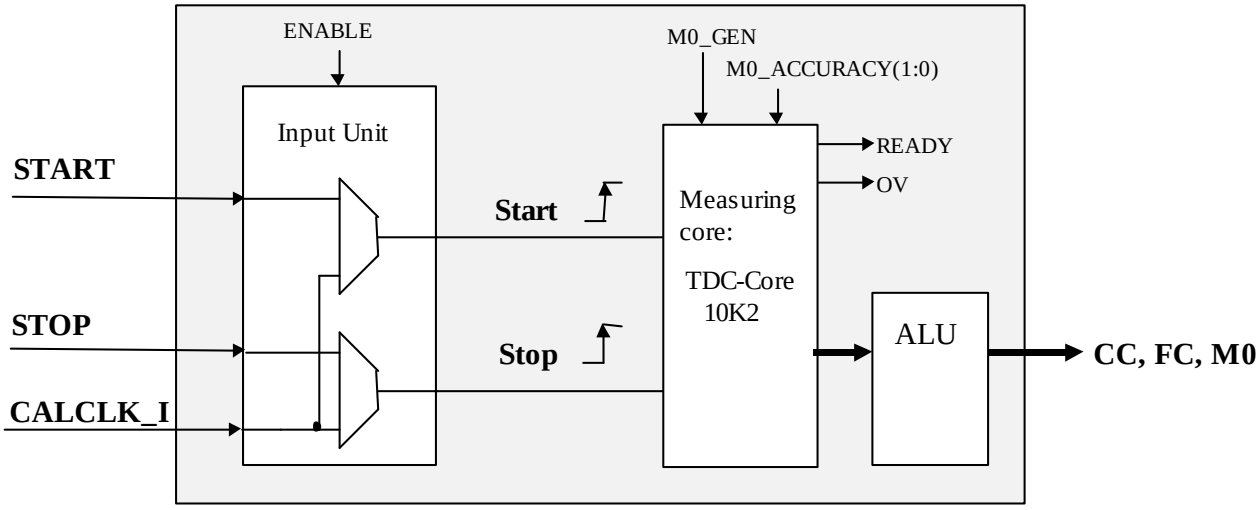


Figure 6.2: Measurement Channel Block Diagram

6.2.1 Input Unit

The input unit handles the incoming start-, stop- and calibration clock-signals. It decides, which signal (START, STOP or CALCLK_I) is passed on as a start- or stop-signal to the measuring core, depending on time or calibration measurement.

If the channel is disabled via the Control Register, no start- or stop-signals will reach the measuring core and no time measurements will take place. During a calibration measurement which has to be executed while the channel is disabled, the channel is enabled automatically for the calibration clock.

6.2.2 Measuring Core

The measuring core of the MPW10K2 is realised as hardmacro **TDC-Core 10K2**. The measuring core determines the time difference between a start- and a stop-signal with a typical resolution of 45ps (5V, 25°C). The measuring core then provides measurement or calibration values in the form of raw values to the ALU for further processing.

In addition, depending on the configuration the measuring core generates the TDC-specific characteristic quantity M0. It can be selected by software, whether M0 is generated with 1-fold, 4-fold, 16-fold or with 32-fold accuracy.

To achieve a high precision accuracy electrical coupling effects can be minimized applying the MPW10K2's separated power supply pins for the measuring core.

6.2.3 Arithmetical Logic Unit (ALU)

The ALU is a flash based ALU. At the end of a time or calibration measurement which is indicated via pin READY and within the Status Register, the ALU calculates the measurement result, consisting of **CC** (Coarsecount), **FC** (Finecount) and, if enabled, **M0** (TDC-specific characteristic quantity). After 10ns (5V, 25°C) the measurement result is accessible via the result registers at the latest.

6.3 MPW10K2 Registers

The MPW10K2 provides one Control Register, three result registers and one Status Register. The registers are accessible via the processor interface (see Chapter 6.4). All registers are readable, the only writeable register is the Control Register. For addressing the registers refer to Chapter 7.1.

6.3.1 Control Register

The width of the Control Register is 8 bit. Here the channel is enabled and disabled, the M0-generation can be suppressed and the M0-accuracy and the division factor of the calibration clock divider are selected. For detailed information on the individual register bits refer to Chapter 7.2.1.

6.3.2 Result Registers

The width of all result registers is 16 bit.

6.3.2.1 CC-Register

The CC-Register contains the Coarsecount CC. For detailed information on the individual register bits refer to Chapter 7.2.2.

6.3.2.2 FC-Register

The FC-Register contains the Finecount FC. For detailed information on the individual register bits refer to Chapter 7.2.3.

6.3.2.3 M0-Register

The M0-Register contains the TDC-specific characteristic quantity M0. For detailed information on the individual register bits refer to Chapter 7.2.4.

6.3.3 Status Register

The width of the Status Register is 8 bit. It reflects the present status of the MPW10K2. The Status Register contains three status flags, which are described in detail in Chapter 6.4.2 and Chapter 7.2.5.

6.4 Processor Interface

Figure 6.3 shows the block diagram of the processor interface. Via the processor interface the access to the Control Register of the MPW10K2 is performed as well as the access to the Status Register and the result registers.

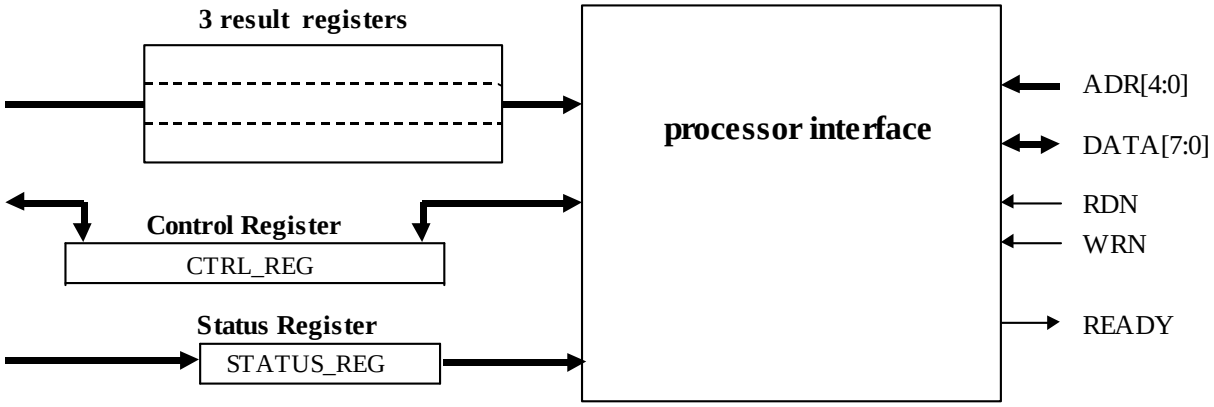


Figure 6.3: processor interface block diagram

In addition to the data- and control lines the processor interface provides the status flag READY for interrupt generation at the connected processor.

6.4.1 Data- and Control Lines

6.4.1.1 Overview

The MPW10K2 provides the following data- and control lines:

- DATA[7:0]: Bi-directional data bus
- RDN: Read strobe (low active)
- WRN: Write strobe (low active)
- ADR[4:0]: Address bus

6.4.1.2 Timing Diagrams

Figure 6.4 and Figure 6.5 show the read and write cycle timings. In Table 6.1 the associated read and write cycle timing characteristics are specified.

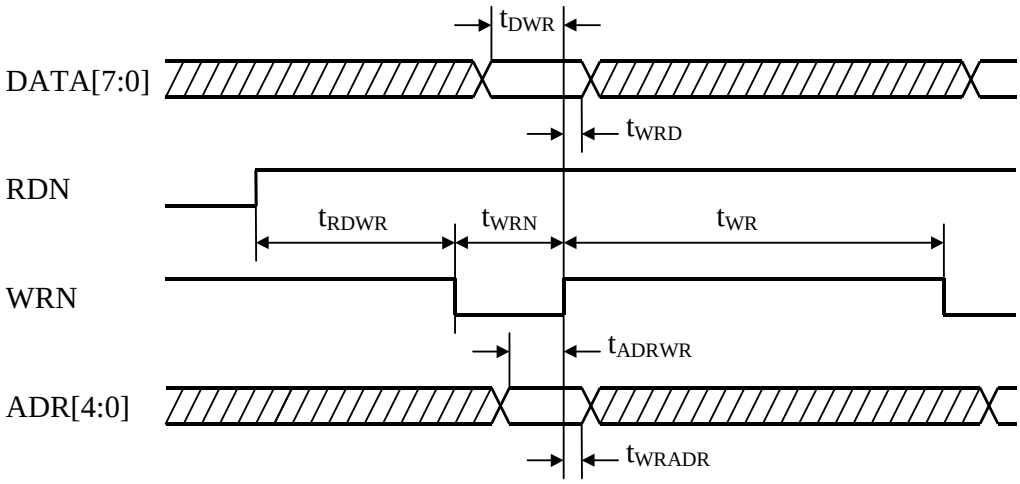


Figure 6.4: Write Cycle Timing

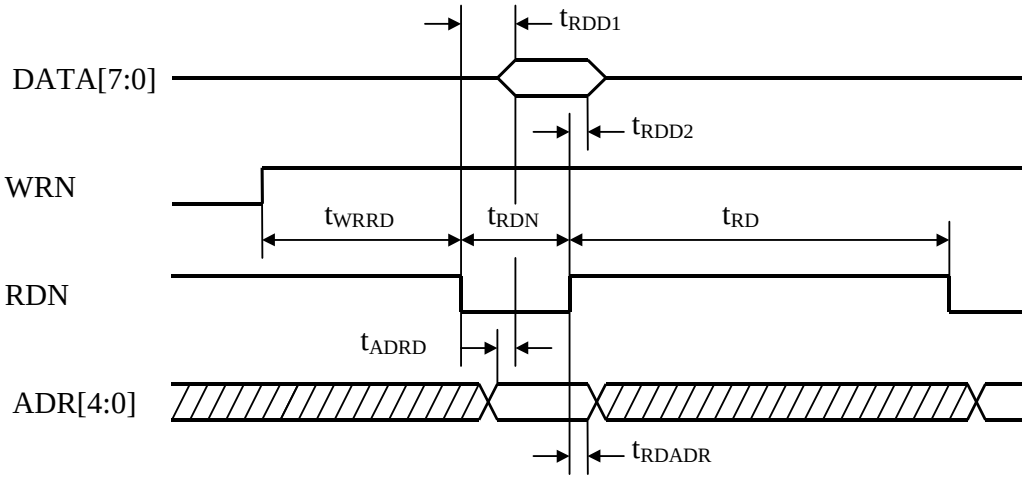


Figure 6.5: Read Cycle Timing

Parameter	Min	Max	Unit
t_{WRN}	25	-	ns
t_{WR}	25	-	ns
t_{DWR}	10	-	ns
t_{WRD}	0	-	ns
t_{ADRWR}	10	-	ns
t_{WRADR}	3	-	ns
t_{RDWR}	25	-	ns

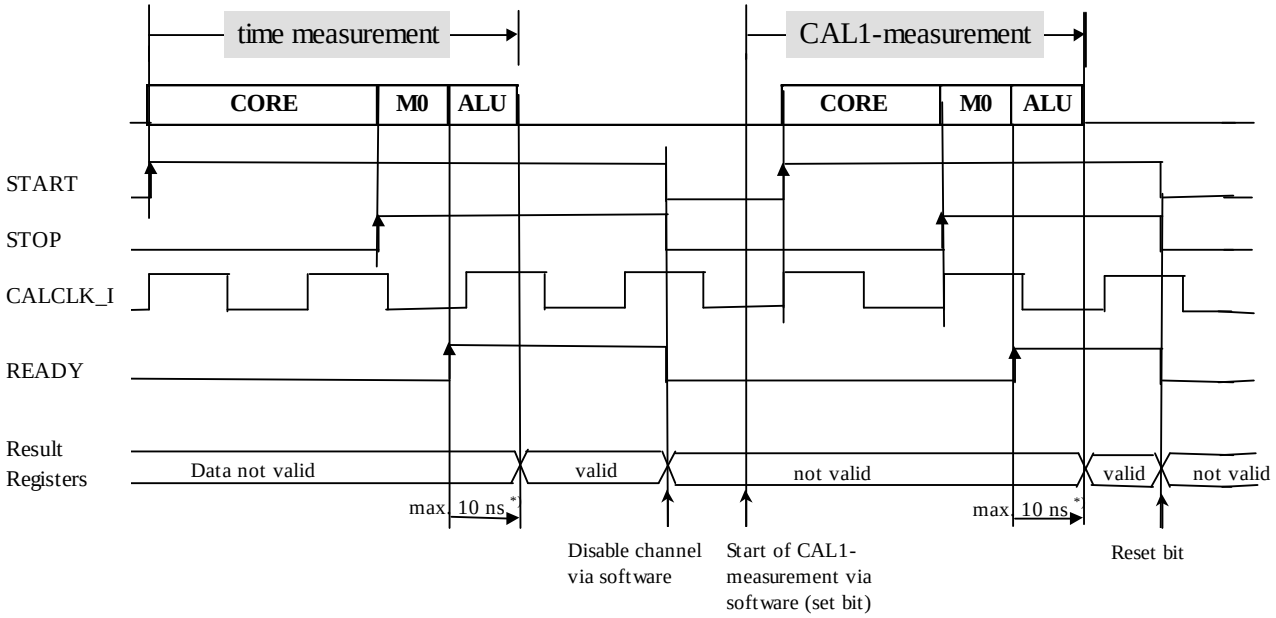
Parameter	Min	Max	Unit
t_{RDN}	25	-	ns
t_{RD}	25	-	ns
t_{RDD1}	-	15	ns
t_{RDD2}	2	12	ns
t_{ADRD}	-	15 *)	ns
t_{RDADR}	3	-	ns
t_{WRRD}	25	-	ns

- V_{DD} = 2.7V – 5.5V, T_A = -40 to +85°C, Load = 30pF
- *) V_{DD} < 3.3V: 25 ns

Table 6.1: Write Cycle and Read Cycle Timing Characteristics

6.4.2 Status Flag READY

The status flag READY is accessible via pin and via the Status Register (see Chapter 7.2.5). Figure 6.6 shows exemplarily the status flag READY during a time measurement cycle and the first part of a calibration measurement cycle (= CAL1-measurement) with M0-generation enabled.



CORE: Measurement in progress
M0: M0-generation
ALU: Calculation of CC, FC and M0

*) - V_{DD} = 5V, T_A = 25°C
- For other conditions refer to Table 8.5: t_{ALU}

Figure 6.6: Status Flag READY

7 Programming of the MPW10K2

Programming the MPW10K2, configuring and reading out the status and measurement results is done via the processor interface. The relevant data is read and written via the bi-directional data bus DATA[7:0]. For addressing the registers, the 5 bit wide address bus ADR[4:0] is used.

7.1 Addressing

In Table 7.1 all register addresses are shown. The Status Register is accessible via two addresses.

Address ADR[4:0]		**Register**		**writeable (w) readable (r)**
hex	**dec**			
0x00	0	---		---
0x01	1	CTRL_REG		w / r
0x02	2	---		---
0x03	3	---		---
0x04	4	---		---
0x05	5	---		---
0x06	6	---		---
0x07	7	---		---
0x08	8	CC_REG	(LowByte)	r
0x09	9	CC_REG	(HighByte)	r
0x0A	10	FC_REG	(LowByte)	r
0x0B	11	FC_REG	(HighByte)	r
0x0C	12	M0_REG	(LowByte)	r
0x0D	13	M0_REG	(HighByte)	r
0x0E	14	STATUS_REG		r
0x0F	15	---		--
0x10	16	---		---
0x11	17	---		---
0x12	18	---		---
0x13	19	---		---
0x14	20	---		---
0x15	21	---		---
0x16	22	---		---
0x17	23	---		---
0x18	24	---		---
0x19	25	---		---
0x1A	26	---		---
0x1B	27	---		---
0x1C	28	---		---
0x1D	29	---		---
0x1E	30	STATUS_REG		r
0x1F	31	---		--

Table 7.1: Register Addresses

7.2 Register Formats

7.2.1 Control Register (CTRL_REG)

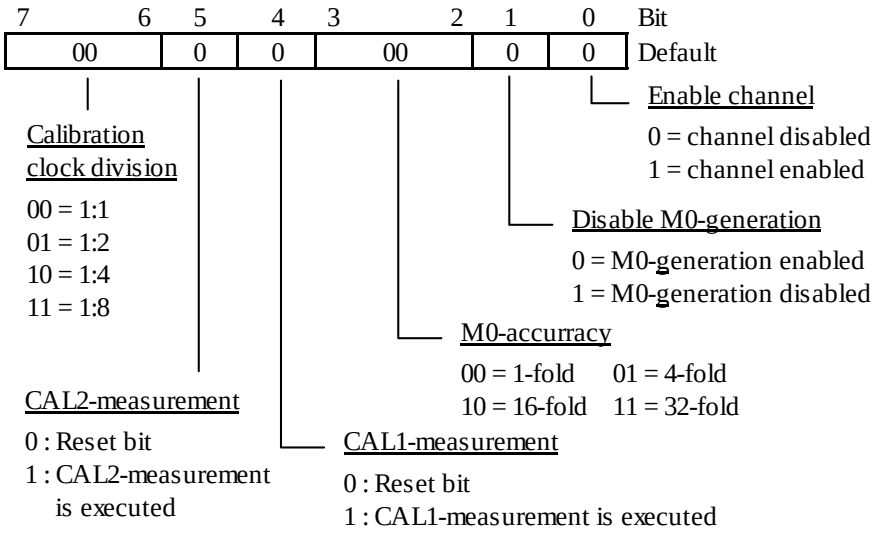


Figure 7.1: Control Register CTRL_REG Format

7.2.2 CC-Register (CC_REG)

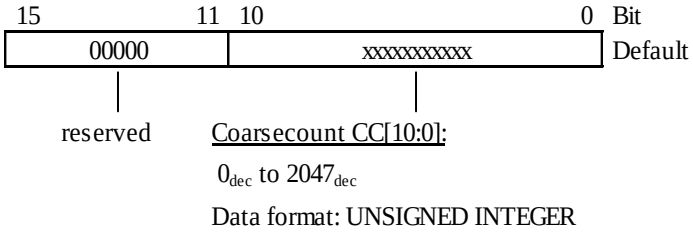


Figure 7.2: CC-Register CC_REG Format

7.2.3 FC-Register (FC_REG)

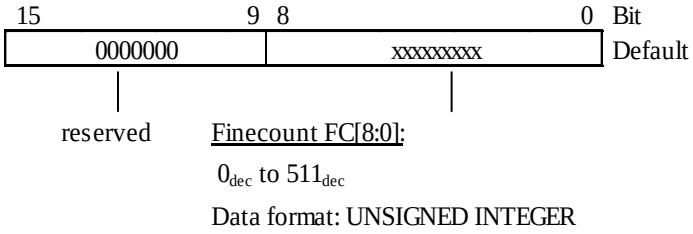


Figure 7.3: FC-Register FC_REG Format

7.2.4 M0-Register (M0_REG)

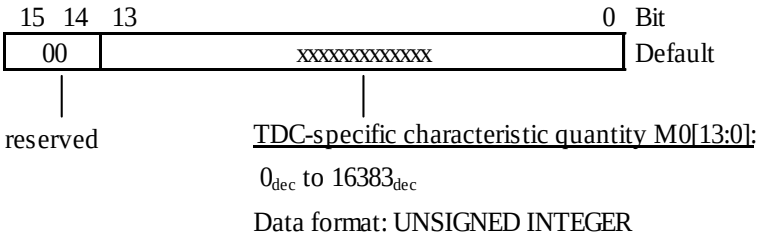
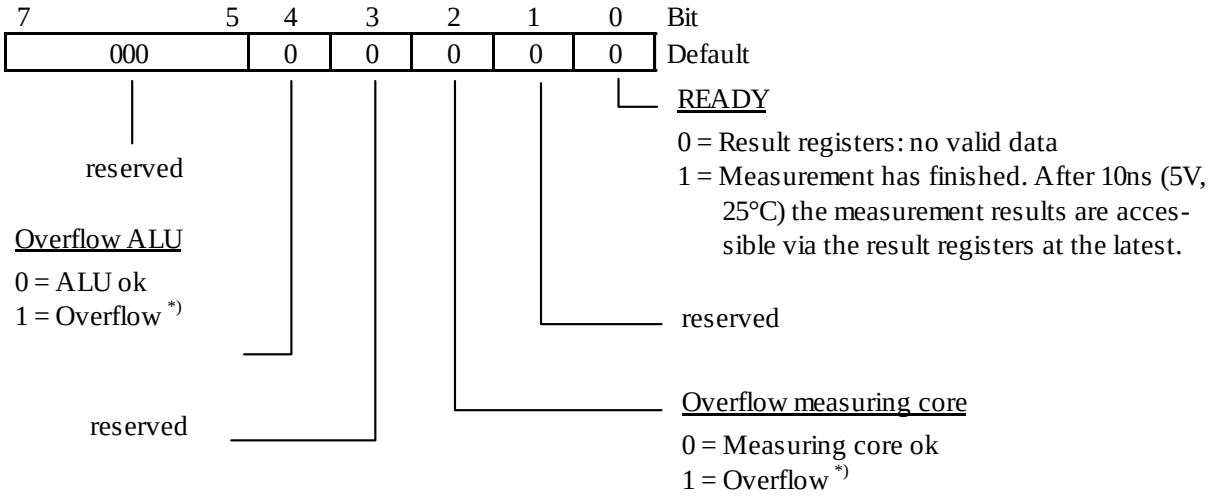


Figure 7.4: M0-Register M0_REG Format

7.2.5 Status Register (STATUS_REG)



*) Overflow is cleared

- on power-on reset
- on reset the Control Register‘s bit0 when time measurement
- on reset the Control Register’s bit4 resp. bit5 when calibration measurement

Figure 7.5: Status Register STATUS_REG Format

8 Appendix

8.1 Electrical Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IL_CMOS}	Input Low Voltage		GND - 0.3		0.3 V_{DD}	V
V_{IH_CMOS}	Input High Voltage		0.7 V_{DD}		V_{DD} + 0.3	V
I_{IN}	Input Current	V_{IN} =V_{DD} or GND	-10		10	µA
V_{OH_CMOS}	Output High Voltage	I_{OH} = -4mA	V_{DD} - 0.8			V
V_{OL_CMOS}	Output Low Voltage	I_{OL} = 4mA			0.4	V
I_{OZ}	3-State Output Leakage Current	V_{OH} = V_{DD} or GND	-10		10	µA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or GND	Design Depend			µA

***NOTE**: Junction temperature range –55°C to +125°C*

Table 8.1: DC Characteristics @ V_{DD} = 5V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IL_CMOS}	Input Low Voltage		GND - 0.3		0.3 V_{DD}	V
V_{IH_CMOS}	Input High Voltage		0.7 V_{DD}		V_{DD} + 0.3	V
I_{IN}	Input Current	V_{IN} =V_{DD} or GND	-10		10	µA
V_{OH_CMOS}	Output High Voltage	I_{OH} = -4mA	V_{DD} - 0.8			V
V_{OL_CMOS}	Output Low Voltage	I_{OL} = 4mA			0.4	V
I_{OZ}	3-State Output Leakage Current	V_{OH} = V_{DD} or GND	-10		10	µA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or GND	Design Depend			µA

***NOTE**: Junction temperature range –55°C to +125°C*

Table 8.2: DC Characteristics @ V_{DD} = 3.3V

Symbol	Parameter	Rating	Unit	Note
V_{DD}	DC Supply Voltage	-0.3 to +7.0	V	
V_{IN}	Input Pin Voltage	-0.3 to V_{DD} + 0.3	V	
I_{IN}	Input Current on any Pin	-100 to +100	mA	25°C
T_{STRG}	Storage Temperature	-65 to +150	°C	
H	Humidity Noncondensing	5 to 85	%	Noncond.
	Electrostatic Discharge	1000	V	R=1.5kOhm, C=100pF
	Lead Temperature	260	°C	T=10s

***NOTE**: Stresses above these values may cause permanent damage to the device.*

Table 8.3: Absolute Maximum Ratings

8.2 Minimum Pulse Width of Start- and Stop-Signals

Table 8.4 shows the minimum pulse width $\mathbf{t_s}$ of signals on the start- and stop-inputs START and STOP for different conditions. The time t_s is relevant for both, high- and low-level of the signals.

Symbol	Description	Min		Typ		Max		Unit
		I	II	I	II	I	II	
t_s	minimum pulse width start / stop	4	5	5	8	8	12	ns

I) V_{DD} = 5V ± 10%, T_A = -40 to +85 °C
II) V_{DD} = 3.3V ± 10%, T_A = -40 to +85 °C

Table 8.4: Minimum Pulse Width of Start- and Stop-Signals

8.3 Dead Times

Due to the measurement principle the MPW10K2 has a dead time $\mathbf{t_{TOT}}$ after the execution of a measurement. Depending on the configuration the dead time differs within a wide range. During dead time the measuring core is disabled because of post-processing and no new measurement will be started within the measuring core.

The dead time of a MPW10K2's time measurement is defined as the minimum time difference between the measurement's stop and the rising edge of WRN when setting the Control Register's bit 0, 4 or 5 to '1' for the next time or calibration measurement.

The dead time of a MPW10K2's calibration CAL1- or CAL2-measurement is defined as the minimum time difference between the rising edge of WRN when starting the measurement by setting the Control Register's bit 4 or 5 to '1' and the rising edge of WRN when setting the Control Register's bit 0, 4 or 5 to '1' for the next time or calibration measurement.

The dead time depends on the following factors:

- period $\mathbf{t_{CALCLK}}$ of the calibration clock CALCLK.
- Division factor **K** of the calibration clock divider.
- Time $\mathbf{t_{M0}}$ for M0-generation with 1-fold accuracy shown in Table 8.5.
- Accuracy factor **A** for M0-generation.
- Time $\mathbf{t_{ALU}}$ for ALU calculations shown in Table 8.5.

Symbol	Description	Min		Typ		Max		Unit
		I	II	I	II	I	II	
t_{ALU}	ALU calculation	6	8	10	14	15	23	ns
t_{M0}	M0-generation	50	65	95	140	165	265	ns

I) V_{DD} = 5V ± 10%, T_A = -40 to +85 °C
II) V_{DD} = 3.3V ± 10%, T_A = -40 to +85 °C

Table 8.5: t_{ALU} and t_{M0}

The dead time contains the so-called communication time $\mathbf{t_{KOM}}$ with the connected processor, because the measurement result has to read out before next measurement.

The time $\mathbf{t_{KOM}}$ is made up as follows:

Readout the result registers: 6 * (t_{RD} + t_{RDN})
Disable channel resp. reset the Control Register's bit 4 or 5 to '0': 1 * (t_{WR} + t_{WRN})
Enable channel resp. set the Control Register's bit 4 or 5 to '1': 1 * (t_{WR} + t_{WRN})

=> (4) $t_{KOM} = 6 * (t_{RD} + t_{RDN}) + 2 * (t_{WR} + t_{WRN})$

The minimum values for t_{RD}, t_{RDN}, t_{WR} and t_{WRN} are listed in Table 6.1.

8.3.1 Dead time of time measurements

The dead time t_{TOT} of time measurements is calculated as follows: *)

(5) $t_{TOT} = (1.8 + A) * t_{M0} + t_{ALU} + t_{KOM}$

8.3.2 Dead time of CAL1-measurements

The dead time t_{TOT} of CAL1-measurements is calculated as follows: *)

(6) $t_{TOT} = 3 * K * t_{CALCLK} + (1.8 + A) * t_{M0} + t_{ALU} + t_{KOM}$

8.3.3 Dead time of CAL2-measurements

The dead time t_{TOT} of CAL2-measurements is calculated as follows: *)

(7) $t_{TOT} = 4 * K * t_{CALCLK} + (1.8 + A) * t_{M0} + t_{ALU} + t_{KOM}$

*) Measurements without M0-generation: A= 0.

8.4 Resolution

8.4.1 How to calculate the Resolution

The TDC-Core 10K2's resolution **RES** is calculated using the divided calibration clock period $\mathbf{t_{CAL1}}$, the calibration values **CAL1** and **CAL2**, **M0** and its accuracy **A**:

(8) $\mathbf{RES = t_{CAL1} * A / [M0 * (CAL2 - CAL1)]}$

M0-accuracy	A
1-fold	1
4-fold	4
16-fold	16
32-fold	32

Example:

- $t_{CAL1} = t_{CALCLK} = 250$ ns
- A = 32
- M0 = 5088
- CAL1 = 36.32054
- CAL2 = 72.44108 => RES = 43.53 ps

8.4.2 Voltage Dependence

Table 8.6 shows the voltage dependence of the resolution at normal conditions (typical process, ambient temperature approx. 25°C), derived from averaging the resolution of several chips.

Voltage V_{DD} [V]	RES [ps]
2,7	63
3,0	57
3,3	53
3,6	50
4,0	46
4,5	43
5,0	41
5,5	40

Table 8.6: Resolution Voltage Dependence ($T_A \approx 25$°C, typ.)

8.4.3 Temperature Dependence

The resolution increases by factors of approx. 0,15 ps/K at 3,3V and approx. 0,11 ps/K at 5V.

8.5 Minimum and maximum Measurement Period

Table 8.7 shows the minimum and the maximum measurement period of the MPW10K2 depending on voltage, temperature and process.

Symbol	Min		Typ		Max		Unit
	I	II	I	II	I	II	
t_{VALmin}	3	5	5	8	10	15	ns
t_{VALmax}	6	7	10	13	20	33	µs

I) V_{DD} = 5V ± 10%, T_A = -40 to +85 °C
II) V_{DD} = 3.3V ± 10%, T_A = -40 to +85 °C

Table 8.7: Minimum and maximum Measurement Period

8.6 Power-On Characteristics

The minimum pulse width of a low active power-on reset pulse connected to pin RSTN is 100µs. Figure 8.1 shows a possible reset circuit (RC-circuit). After power-on reset the MPW10K2 is in the default state and has to be configured as shown in the general measurement cycle flow of Chapter 5.

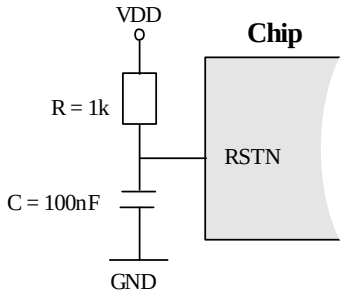


Figure 8.1: Reset Circuit

8.7 Current Consumption TDC-Core 10K2

- 5V, 25°C, typ. process:

  During a measurement (between start and stop event) the current consumption of the measurement core is approx. **6,6mA**. After stop the current consumption is approx. **19,2mA** for a duration of "(1.8 + A) * t_{M0}" (see Chapter 8.3).

- 3,3V, 25°C, typ. process:

  During a measurement (between start and stop event) the current consumption of the measurement core is approx. **2,6mA**. After stop the current consumption is approx. **8,3mA** for a duration of "(1.8 + A) * t_{M0}" (see Chapter 8.3).

8.8 Measurement Results

8.8.1 Differential Non-Linearity

The quality of a measurement not only depends on the TDC's resolution but also on its so called *differential non-linearity (DNL).* The DNL is a criterion for the variation of the quantisation stage's width (LSB-width).

Figure 8.2 shows a typical histogram of the TDC-Core 10K2's LSB-widths at V_{DD} = 5V. The LSB-widths recur every 11 LSBs. The average LSB-width is identical with the resolution. Furthermore the figure illustrates the definition of the DNL.

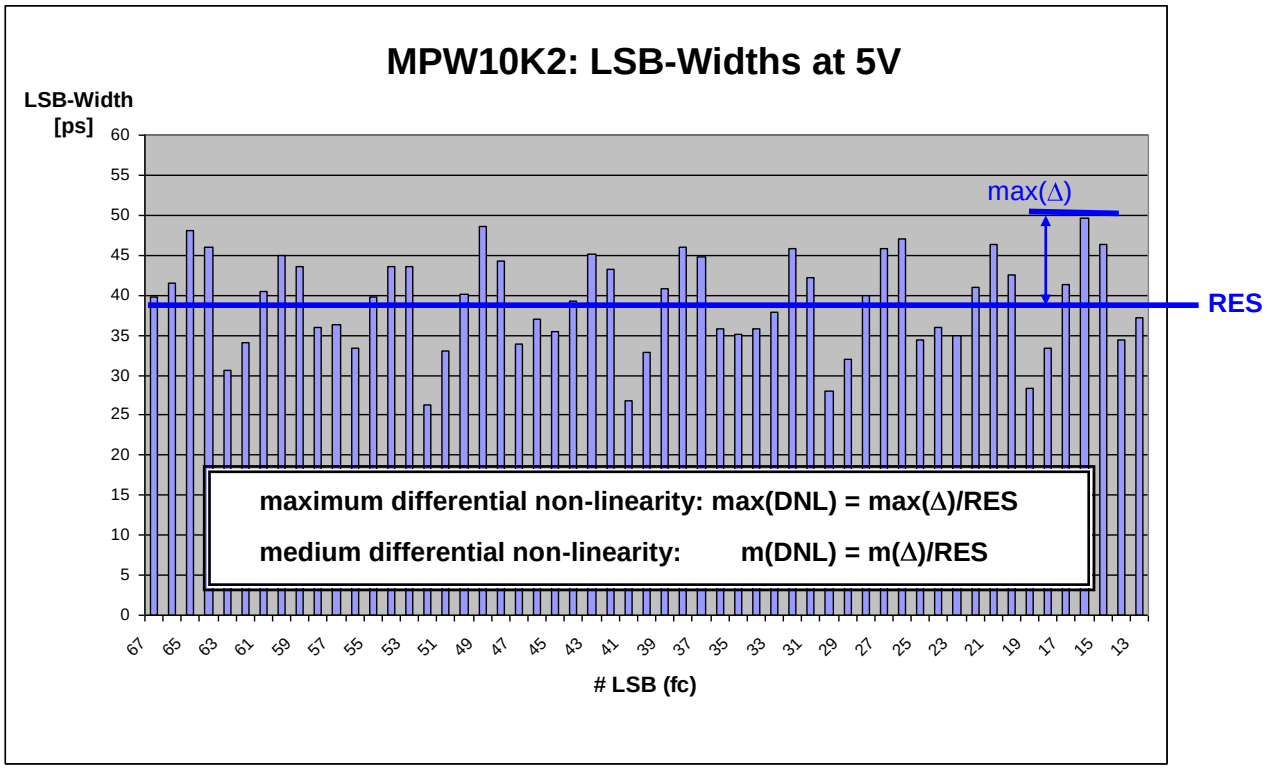


Figure 8.2: Resolution, LSB-Width and Differential Non-Linearity

Table 8.8 shows the *maximum differential non-linearity* **max(DNL)** and *the medium differential non-linearity* **m(DNL)**, based upon measurements of several MPW10K2's at V_{DD} = 5V and 3,3V.

RES [ps] @ 5V	m(DNL) @ 5V	max(DNL)	RES [ps] @ 3,3V	m(DNL) @ 3,3V	max(DNL)
40	14%	35%	52	16%	41%

Table 8.8: Maximum and medium differential Non-Linearity

8.8.2 Standard Deviation

Table 8.9 shows the *maximum standard deviation* **max(Std)** and the *medium standard deviation* **m(Std)** for measurements at the conditions below. The values are averaged and derived from measurements on several chips.

- Measurement period: 150 – 600ns.
- Increment: 1 ns.
- Sampling rate: 50 time measurements per measuring point.
- Calibration clock = 4 MHz.
- 1 calibration measurement (CAL1- + CAL2-measurement) per time measurement.
- Supply voltage: 3.3V and 5V.
- M0-accuracy: 16-fold.
- Temperature: approx. 28°C.
- Reference measurements: Universal Time Interval Counter SR620 (Stanford Research Systems) with a standard deviation of max(Std) = 46ps and m(Std) = 32ps.

RES [ps] @ 5V	Std @ 5V [ps] max	[LSB]	[ps] m	[LSB]
40	39	1.0	24	0.6

RES [ps] @ 3.3V	Std @ 3.3V [ps] max	[LSB]	[ps] m	[LSB]
52	45	0.9	26	0.5

Table 8.9: Standard Deviation

Figure 8.3: Standard Deviation at 5V shows exemplarily a MPW10K2's standard deviation at 5V.

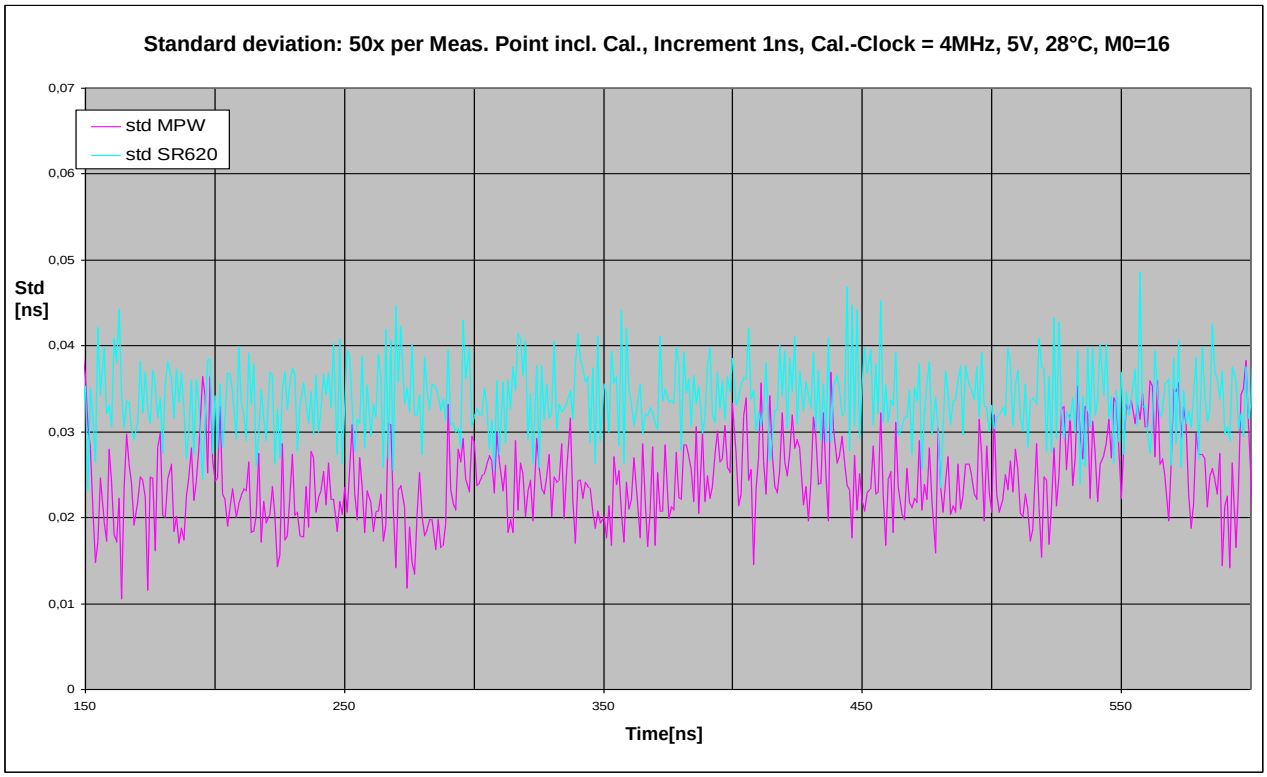


Figure 8.3: Standard Deviation at 5V

8.8.3 Singleshot Measurement Errors

Table 8.10 shows the time-based *singleshot measurement errors* "**σ [ps]**" and the resolution-based errors "**σ [LSB]**". All errors are averaged values derived from measurements on several chips at the conditions given below. In a normal distribution the so called one-sigma area ±σ contains about 68,3% of the measurement results. About 95,5% will fall within the two-sigma area ±2σ.

- Measurement period: 200 - 500ns.
- Increment: 1ns.
- Sampling rate: One time measurement per measuring point.
- Calibration clock = 4 MHz.
- 1 calibration measurement (CAL1- + CAL2-measurement) per time measurement.
- Supply voltage: 3.3V and 5V.
- M0-accuracy: 16-fold.
- Temperature: approx. 28°C.
- Reference measurements: Universal Time Interval Counter SR620

RES [ps] @ 5V	[ps] σ @ 5V	[LSB]	RES [ps] @ 3,3V	[ps] σ @ 3,3V	[LSB]
40	55	1.4	52	70	1.4

Table 8.10: Singleshot Measurement Errors

Figure 8.4 shows exemplarily the measurement errors of singleshot measurements at 5V. The offset of the diagram is approx. 250ps. This systematic error results from a different length of cables for start and stop and is irrelevant here.

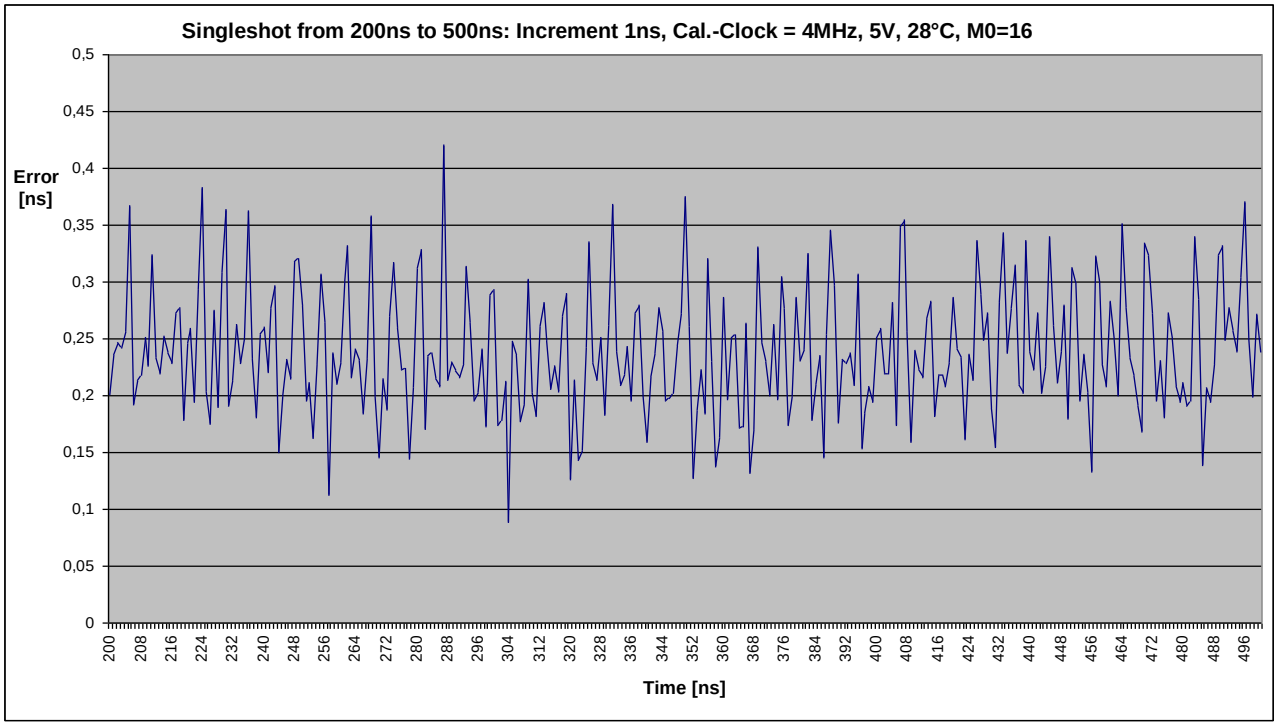


Figure 8.4: Measurement Errors of Singleshot Measurements at 5V

8.8.4 Systematic Error

Due to the measuring principle the TDC-Core 10K2 has a systematic error, shown in Figure 8.5.

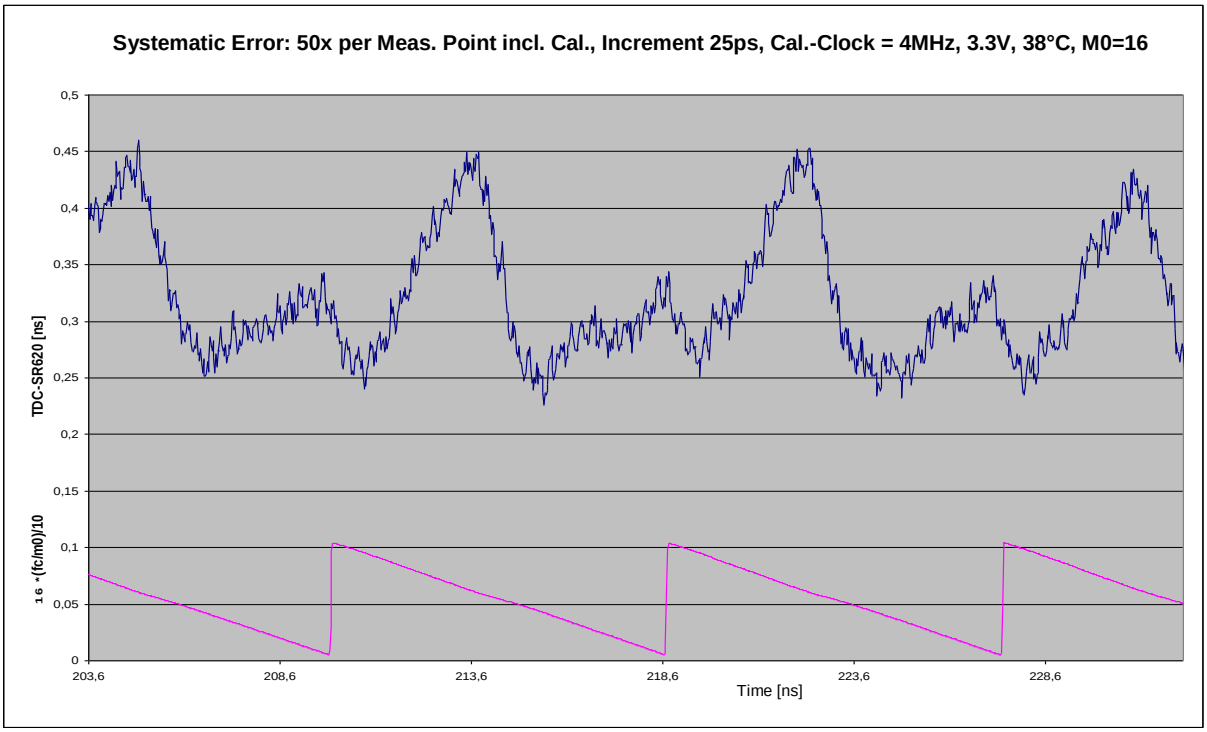


Figure 8.5: Systematic Error at 3.3V

The systematic error is periodical with the fractional portion 'A*fc/m0' of the measurement value (see formula 1 in Chapter 4.3). The periodicity is shown once more in Figure 8.6.

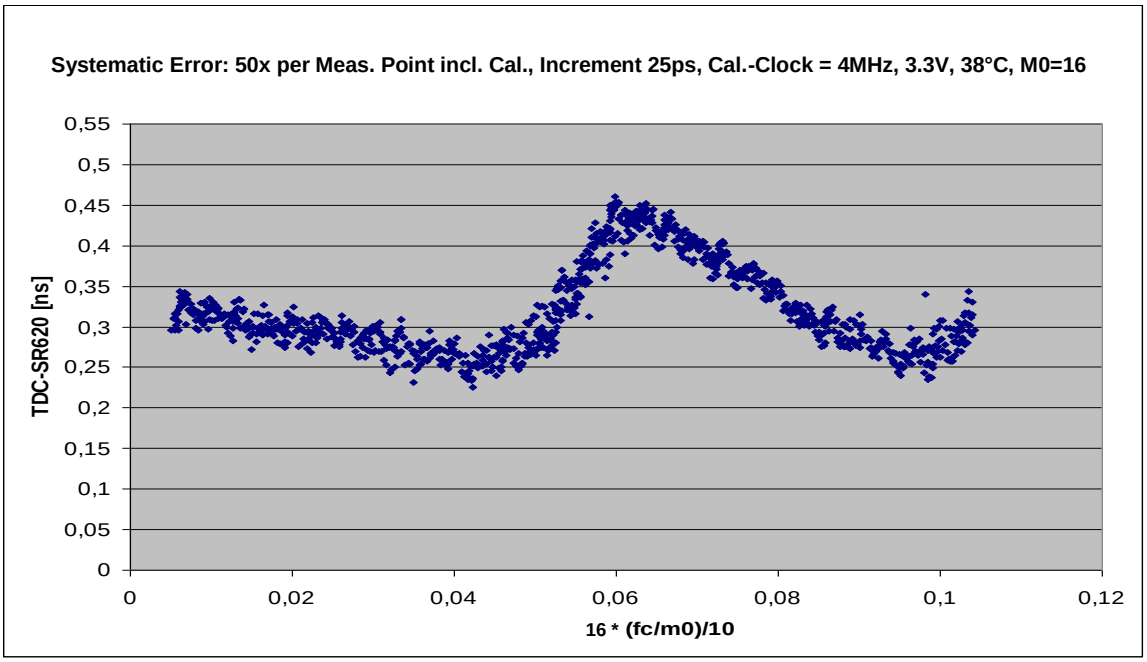


Figure 8.6: Periodicity of the Systematic Error at 3.3V

Table 8.11 shows the peak-to-peak values of the systematic error. All values are averaged and derived from measurements on several chips.

Supply Voltage [V]	Resolution [ps]	Peak-to-Peak [ps]	Peak-to-Peak [LSB]
5	40	195	4,9
3,3	52	225	4,3

Table 8.11: Systematic Error: Peak-to-Peak Values

Remark:

Including the systematic error in the calculations of measurement and calibration values (see Chapter 4.3) the singleshot measurement errors (see Chapter 8.8.3) for instance, can be much reduced.